

# Elio Karkar

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## Education

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University of California, Santa Cruz

Graduation: June 2025

Bachelor of Science in Computer Engineering

Relevant coursework: VSLI, System Verilog, Embedded System Design, Operating Systems, Logic Design, Data Structures and Algorithms, Artificial Intelligence, Python, C/C++, Java

## Skills & Achievements

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Skills: C/C++, Python, debugging, Linux, shell scripting (Bash, Perl, TCL), configuration management, code review, algorithms and data structures, Rust, hardware/software co-design

Tools/Frameworks/Hardware: Linux, Git, CMake, AWS, FPGA, Vivado, OpenLane, Openroad, Yosys, Verilator, SVN, Angular, SCL, LaTeX

Achievements: Dean's Honor Roll, Spring 2025

## Experience

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Qovo Solutions – Network Support Technician

Winter 2024 – Spring 2025

Morgan Hill, CA

- Deployed and configured Avigilon IP camera systems across 25+ commercial and institutional sites in **Linux**-based environments.
- Diagnosed and resolved complex system and **network** issues using **Wireshark**, improving reliability and uptime across deployments.
- Administered IP configurations, **VLAN** setup, and port-forwarding rules on **Linux**, validating changes through **regression testing**.
- Engineered a software-defined router using POX and Mininet, simulating large-scale environments to validate traffic control logic.
- Developed and enforced **TCP/UDP**-based traffic control policies, improving segmentation and overall system robustness.

Slugmatch Alumni Platform – Backend Developer

Fall 2024

UC Santa Cruz Alumni Association

- Contributed to the architecture and implementation of backend services for Slugmatch, a live alumni engagement platform supporting large-scale user connectivity. (<https://slugmatch.app>)
- Designed and integrated REST and GraphQL APIs using **Python** and **C/C++**, validated through **unit** and **integration testing**.
- Implemented AWS services (Lambda, DynamoDB, S3, AppSync) to deliver scalable infrastructure.
- Enhanced reliability through **unit testing**, **code review**, and **CI/CD**-style workflows using Git-based automation.

## Projects

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Floating Point Adder Optimization

Spring 2025

- Optimized IEEE-754 combinational floating-point adder to improve FPGA timing performance.
- Increased operating frequency by 312% (from 8 MHz to 33 MHz) through pipeline tuning and logic restructuring.
- Used **Verilator** and DPI-C for fuzz testing, **correctness validation**, and **regression testing**.
- Synthesized design with Yosys/Nextpnr toolchain for iCEBreaker FPGA.

FPGA Hardware Labs

Spring 2025

- Designed FIFO, RAM-based buffers, and ready/valid pipelines in SystemVerilog.
- Built and tested pipelined adder/multiplier/MAC units with timing-aware design practices.
- Verified functionality using **Verilator-based simulation** and maintained reusable **source code** for **regression testing**.

ESP32-C3 Audio Tuner

Spring 2025

- Designed and implemented a real-time audio tuner on the ESP32-C3 microcontroller using **embedded C/C++**.
- Implemented a lightweight frequency analysis pipeline to achieve  $\pm 1$  Hz pitch detection accuracy under real-time constraints.
- Optimized performance through efficient C++ routines and systematic **troubleshooting** for low-latency execution.

ESP32-C3 Bluetooth Mouse

Winter 2025

- Built a wireless Bluetooth HID mouse using the ESP32-C3 microcontroller and **ESP-IDF**, validated through **system-level testing**.
- Interfaced an ICM-42670-P accelerometer over I2C and validated behavior across **Linux** and **macOS** hosts.